HIGH ELECTRON MOBILITY TRANSISTOR HAVING REDUCED THRESHOLD VOLTAGE VARIATION AND METHOD OF MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority under 35 U.S.C. §119 to Korean Patent Application No. 10-2011-0107057, filed on Oct. 19, 2011, and Korean Patent Application No. 10-2012-0059433, filed on Jun. 1, 2012 in the Korean Intellectual Property Office, the disclosure of each of which is incorporated herein in its entirety by reference.

BACKGROUND

1. Field

Example embodiments relate to a power device and/or a manufacturing method thereof, and for example, to a high electron mobility transistor having reduced threshold voltage variation and/or a method of manufacturing the same.

2. Description of the Related Art

A high electron mobility transistor (HEMT) may include compound semiconductors having different polarizabilities. A 2-dimensional electron gas (2DEG) may be formed in a channel layer and used as a carrier. When a HEMT includes a thick AlGaN barrier layer, the concentration of 2DEG in a channel layer may increase so that a current during turn-on, that is, an ON current, may increase. Yet, when the thickness of the AlGaN barrier layer is thick, a degree of an energy band of the AlGaN barrier layer being raised by a depletion layer formed between a gate and the AlGaN barrier layer is small. Thus, the 2DEG may not be completely removed from the channel layer under the gate so that an operation of an enhanced mode (E-mode) of the HEMT may be difficult.

Some HEMTs include a recess in the AlGaN barrier layer under the gate. However, the thickness of the AlGaN barrier layer remaining under the recess may vary in an etch process to form the recess. Accordingly, the thickness of the AlGaN barrier layer remaining under the recess may be different for each HEMT. Accordingly, a threshold voltage Vth for turn-on may vary for each HEMT.

SUMMARY

Example embodiments relate to a high electron mobility transistor (HEMT) having reduced threshold voltage variation.

Example embodiments relate to a method of manufacturing a HEMT.

Additional aspects will be set forth in part in the description which follows and, in part, will be apparent from the description, or may be learned by practice of example embodiments.

According to example embodiments, a high electron mobility transistor includes a substrate, a channel layer on the substrate, the channel layer including a 2DEG channel configured to generate a two-dimensional electron gas and a depletion area, a first channel supply layer on the channel layer, the first channel supply layer corresponding to the 2DEG channel and defining an opening that exposes the depletion area, a depletion layer on the first channel supply layer and on the depletion area of the channel layer, a second channel supply layer between the depletion layer and the depletion area, source and drain electrodes spaced apart on the first channel supply layer, and a gate electrode on the depletion layer.

The depletion layer may be one of contacted to and separated from at least one of the source and drain electrodes.

An insulation layer may be between the gate electrode and the depletion layer.

A polarizability of the depletion layer may be less than a polarizability of the first channel supply layer. The depletion layer may include a compound semiconductor layer doped with a p-type dopant.

A polarizability of the depletion layer may be less than a polarizability of the first channel supply layer. A concentration of a polarization generation component may vary according to a thickness of the depletion layer.

The first channel supply layer may contain an n-type dopant and may include at least one of aluminum (Al), gallium (Ga), and indium (In).

A thickness of the first channel supply layer may be about 20 nm to about 200 nm.

A polarizability of the second channel supply layer may be less than a polarizability of the first channel supply layer.

The depletion layer may include at least one of aluminum (Al), gallium (Ga), and indium (In).

The first and second channel supply layers may be compound semiconductor layers having the same elements but different composition ratios.

A thickness of the first channel supply layer may be about 20 nm to about 200 nm, and a thickness of the second channel supply layer may be about 5 nm to about 20 nm.

The first and second channel supply layers may have the same polarizability.

The gate electrode may be a metal or a nitride.

The first and second channel supply layers may have the same polarizability.

According to example embodiments, a method of manufacturing a transistor includes forming a channel layer on a substrate, forming a first channel supply film on the channel layer, the first channel supply film having a polarizability greater than a polarizability of the channel layer, forming a first channel supply layer by removing a part of the first channel supply film, the first channel supply layer defining an opening that exposes a depletion area of the channel layer, forming a second channel supply layer on the first channel supply layer and in the opening, forming a depletion layer on the second channel supply layer, forming source and drain electrodes spaced apart on the first channel supply layer, and forming a gate electrode on the depletion layer.

The method may further include forming an insulation layer between the gate electrode and the depletion layer.

A polarizability of the depletion layer may be less than a polarizability of the first channel supply layer. The depletion layer may include a compound semiconductor layer doped with a p-type dopant.

A polarizability of the depletion layer may be less than a polarizability of the first channel supply layer. A concentration of a polarization generation component of the depletion layer may vary according to a thickness of the depletion layer.

The first channel supply layer may contain an n-type dopant and include at least one of aluminum (Al), gallium (Ga), and indium (In).

The depletion layer may include at least one of aluminum (Al), gallium (Ga), and indium (In).